

FIG. 1A

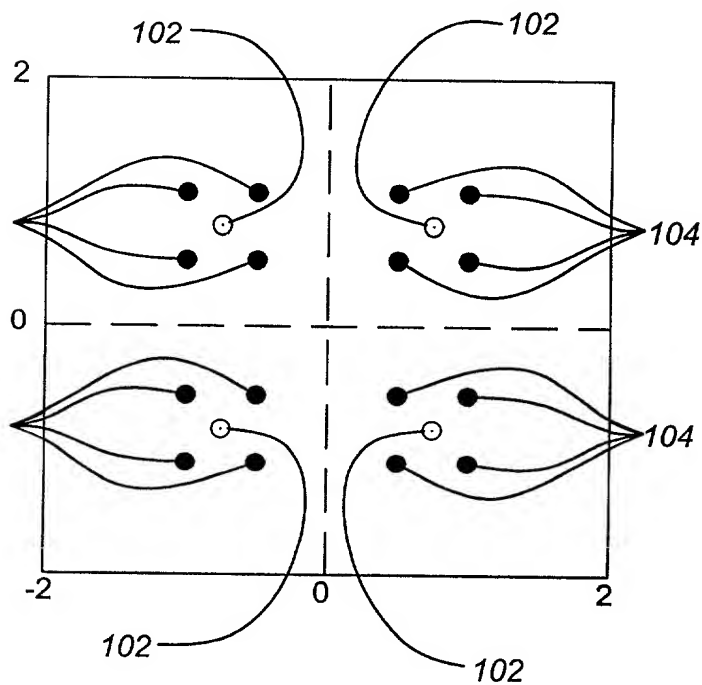
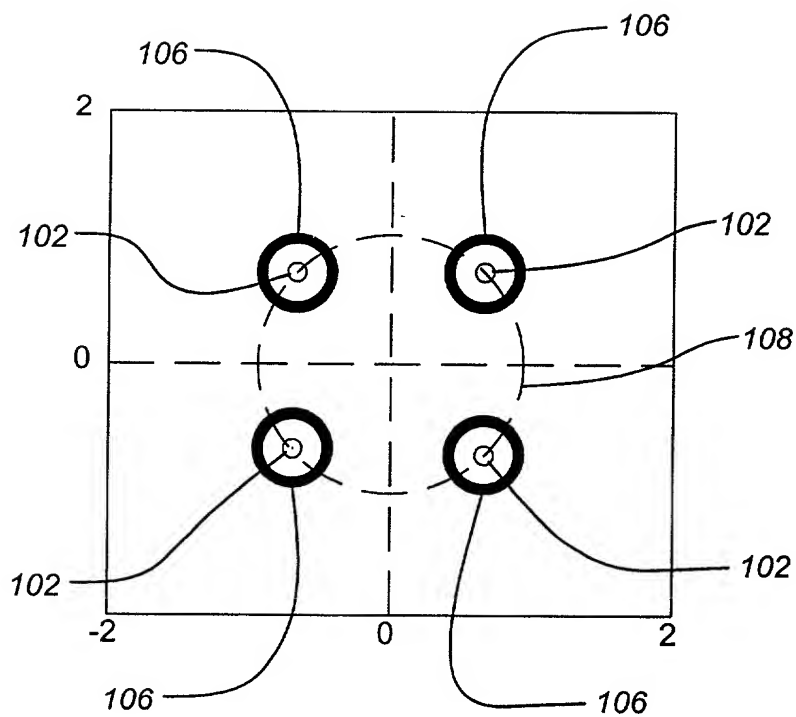


FIG. 1B



**FIG. 1C**

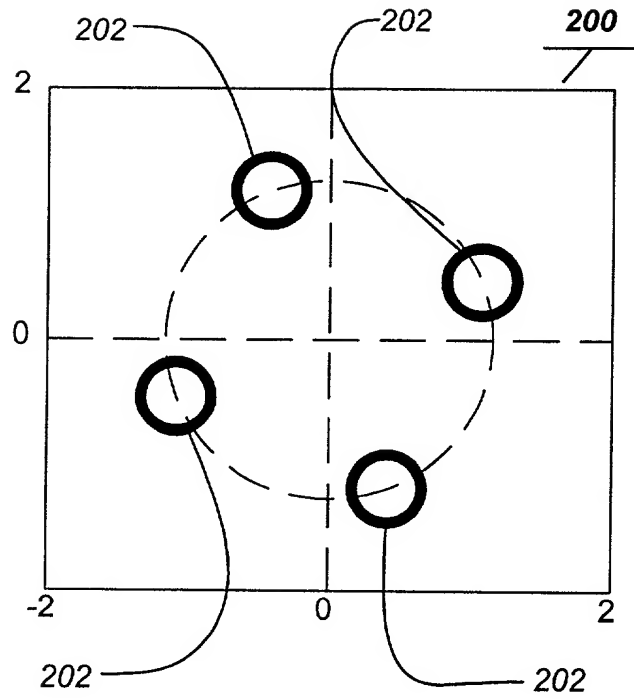


FIG. 2A

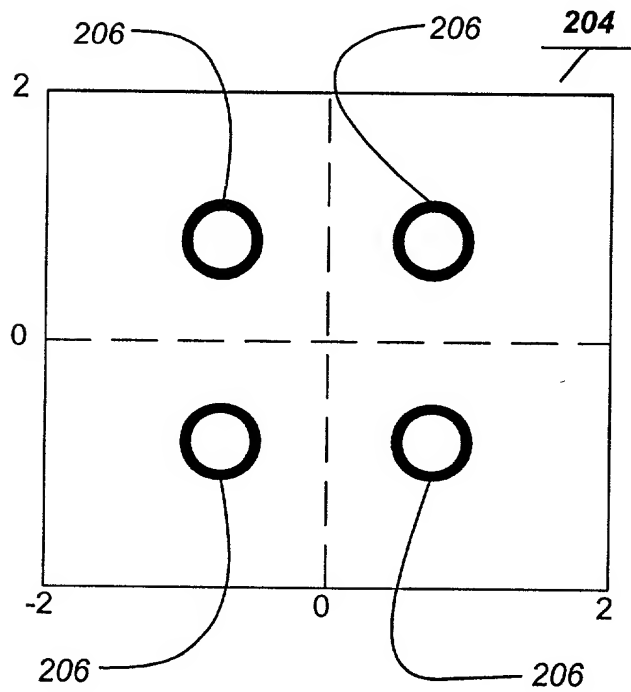


FIG. 2B

US  
Patent  
and  
Trademark  
Office

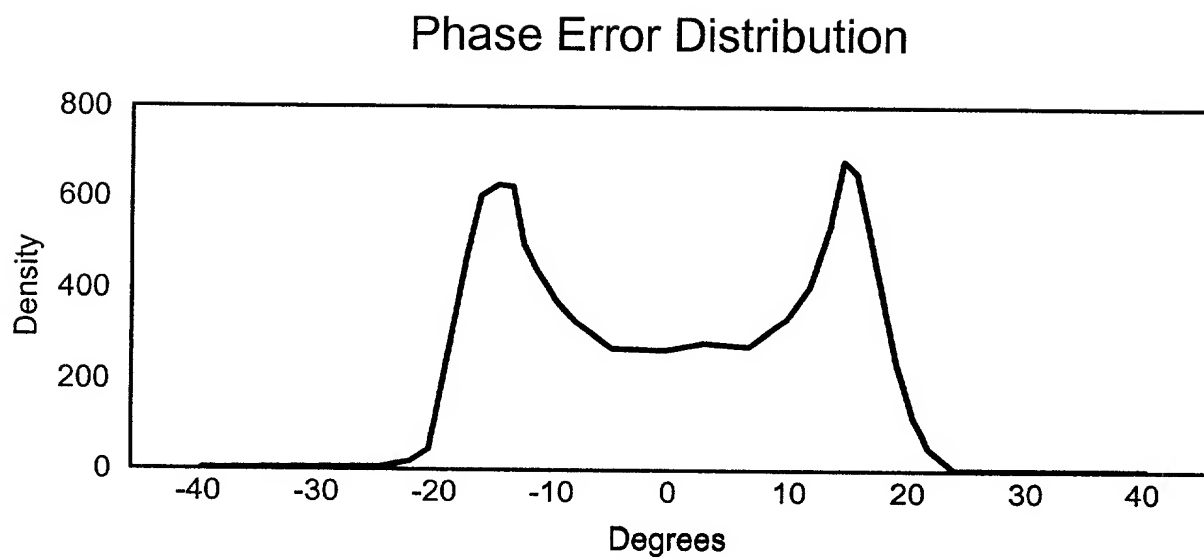


FIG. 2C

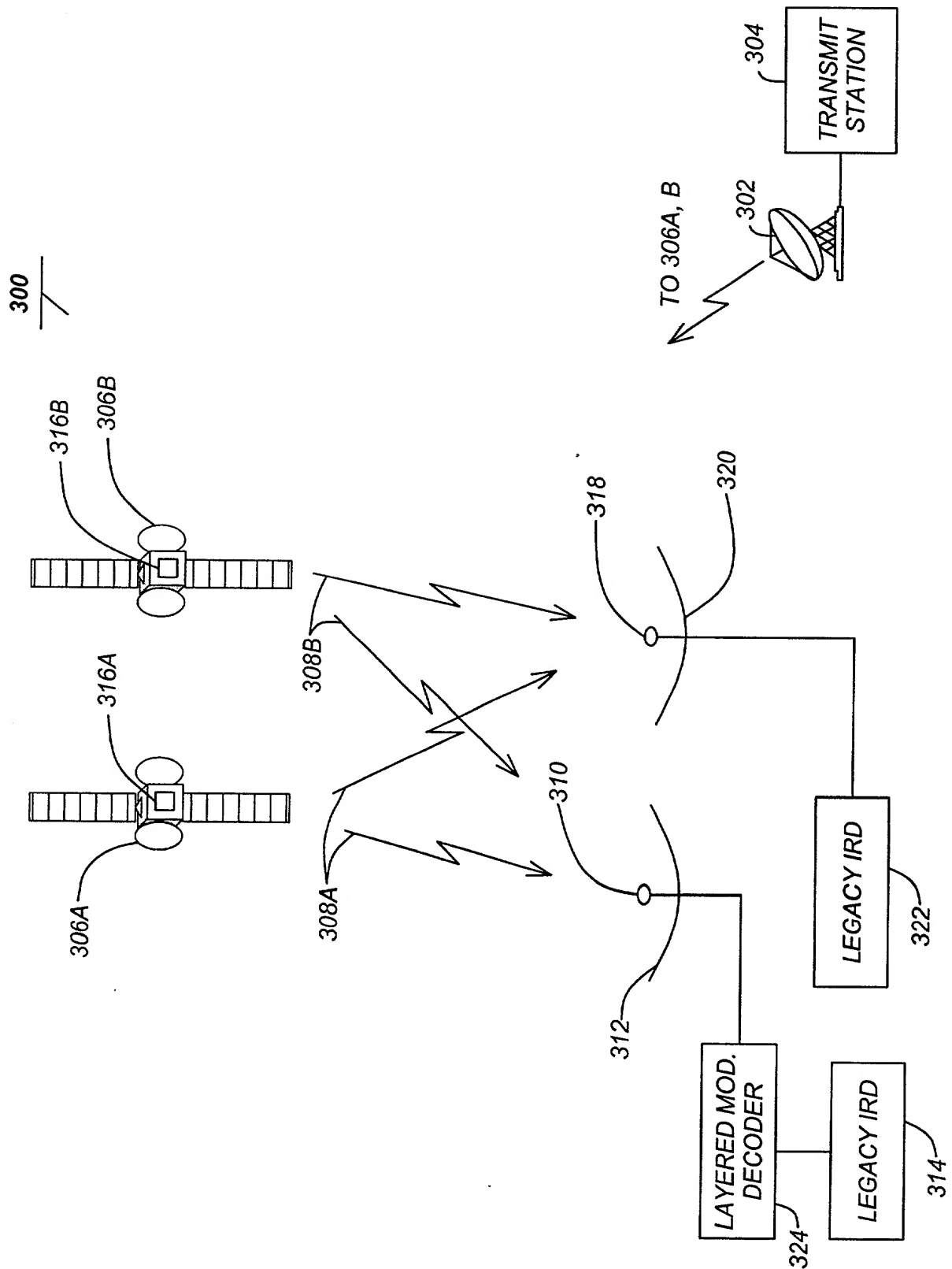


FIG. 3

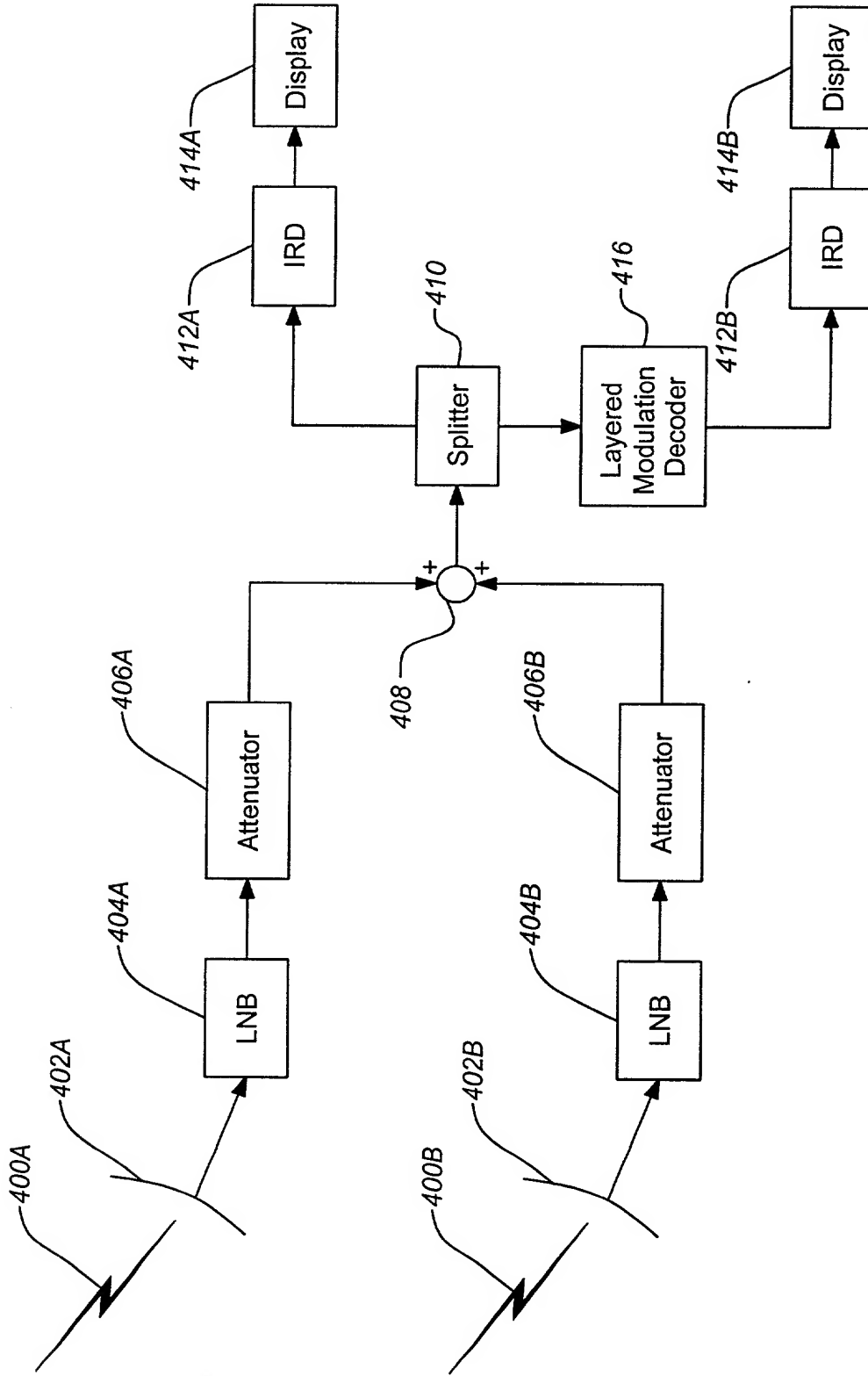


FIG. 4

FIG. 5 is a block diagram of a receiver system 416. The receiver system 416 includes a Tuner 500, LP Filters 502, Dual ADC 504, Freq. Acq. 508, FIR Filter 510, Demod TRL/CRL 512, FEC Decode 514, FEC Encode 516, FIR Filter 518, AM/AM AM/PM LUT 520, Apply AM/AM AM/PM maps 522, AM/AM AM/PM LUT 520, Apply M, phi coeff. 524, FIR Filter 526, Generate M, phi coeff. 528, Delay 530, FIR Filter 532, Delay 534, Delay 536, Dual DAC 540, LP Filters 542, and Mod. 544. The receiver system 416 is configured to receive a signal and process it through various stages including frequency acquisition, demodulation, error correction, and modulation.

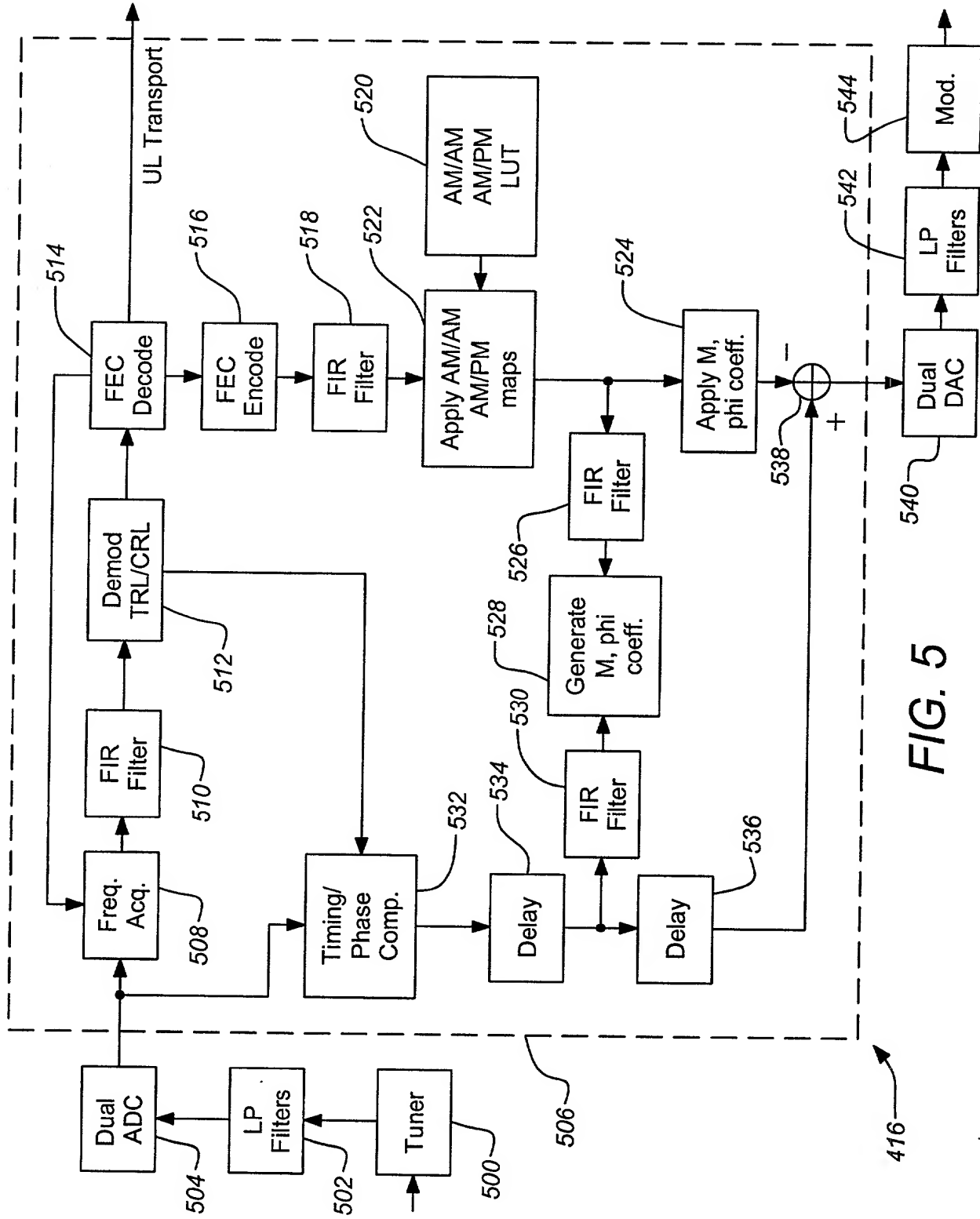
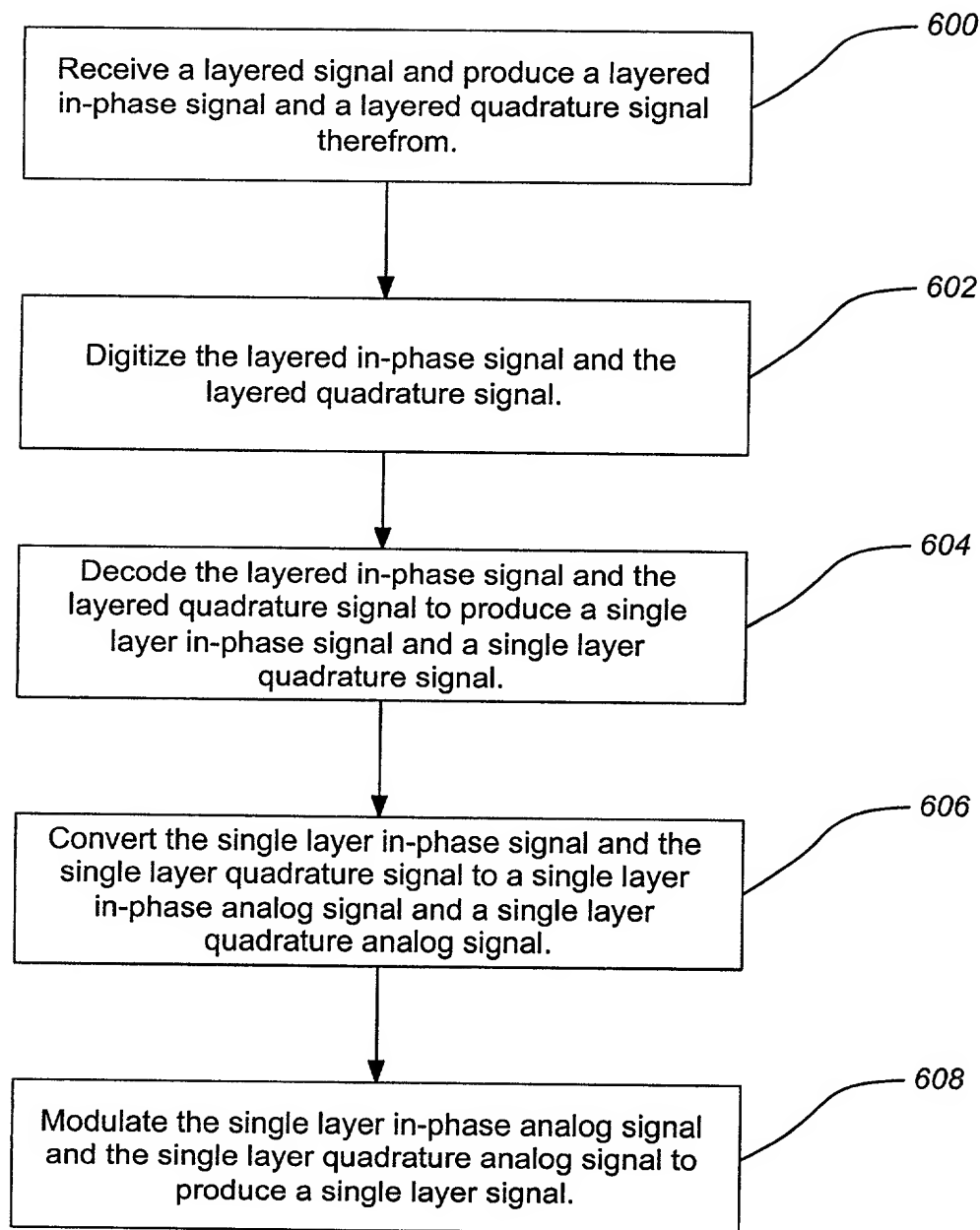


FIG. 5



**FIG. 6**